Abstract of the Disclosure

An on-chip multiprocessor having a chip layout for efficient multiprocessor control, wherein multiple processors and shared portions such as shared caches are symmetric with respect to a desired linear axis and a multiprocessor controller is located in the area containing said linear axis. This makes the distances between the processors and the controller equal and shorter, and also decreases differences in the distance between the controller and shared portions, thereby permitting higher speed processing of signals among these.